AASHISH MITTAL

Head of Engineering
Vice president (Signitude)

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PROFESSIONAL SUMMARY

- **Results-driven Engineering leader with 26+ years** of experience in IP Design & Verification, DAIP Design & Verification, SoC Functional Verification, and Tester Debugging for automotive, consumer, and wireless applications.
- **17+ years of SoC verification expertise** using UVM testbenches and VIPs (ARM & DSP) for complex architectures in automotive, consumer, and wireless applications.
- Built and led **Global Digital MSIP Group**, focusing on **DAIP design, AMS & RTL verification** across multiple nodes (5nm, 16FFC, C28, C40).
- Developed **advanced verification methodologies**: DNG Traceability, RTL & UVM TB Generator, and Automated Verification Compliance Checks.
- **Expertise in defining and developing robust testbench architectures,** driving SoC-level verification to meet logic freeze and tape-out requirements.
- **Pioneered advanced SoC and functional tester verification techniques** to enhance efficiency and reduce test time. Drove the development of state-of-the-art verification methodologies, optimizing processes for improved performance and quality.
- Experience in DFT architecture, IP coding and Timing analysis
- **12+ years** of leadership experience, driving cross-functional collaboration, customer engagement, and high-impact verification strategies.
- Extensive experience in **talent development, university partnerships, and hiring** through **NXP's campus connect & WIN program**
- Visiting professor in **VIT Vellore, SRM** and many other universities of repute
- **Customer-focused and results-driven**, with strong problem-solving, adaptability, and time management skills in dynamic, fast-paced environments.

EXPERTISE & SKILLS

- **SoC Verification & IP Verification and IP coding :** End-to-end IP development from architecture to post-silicon debug, driving verification compliance and automation.
- **MSIP Design & Verification:** Digital IP development (FIR filters, ADC interfaces, clocking IPs) with ISO 26262 compliance for automotive & consumer applications.
- **Advanced Verification Methodologies:** Expertise in UVM, VIP development, assertion-based & formal verification, GLS, AMS, and traceability.
- **Low Power & Flash-based Design**: Specialized in low-power architectures, Flash & Non-Flash designs across 5nm to C90 nodes.
- **Protocol & Interface Debugging:** Strong expertise in AHB, AXI, IPS, APB, CAN, USB, QSPI, NFC, USD, and post-silicon validation.
- **Test & Qualification:** Defined and verified functional test architectures for SoC and tester-level qualification.
- **Innovation & Process Optimization:** Developed automated verification compliance checks and test time reduction strategies.
- **Multiple Tape-outs & Silicon Validation:** Hands-on experience in RTL design, silicon bring-up, and validation across auto, wireless, consumer, and industrial sectors.

PROFESSIONAL EXPERIENCE

Signitude I April 2026 – Present (**Vice President - Head of Engineering)** – Take care semiconductor services and Inhouse Turnkey projects

Incise Semiconductor I 2025 – March 2026 (Senior Engineering Director - Head of India R & D) – Take care semiconductor services

NXP Semiconductors | 1999 – 2025 (Started as a fresher in Motorola, continuing through Freescale & NXP as a Director verification)

Key Assignments Handled:

NXP Semiconductors *(June 2021 – Present)*
Lead IP Design & Verification Engineer (Infrastructure & Serial Digital IPs)

- Spearheading digital IP development, covering architecture requirements, design, verification sign-off, pre/post-silicon debug, and quality assurance.

- Established NXP NXDS flow and implemented automated verification compliance checks, ensuring database sanity and robust quality control.
- Developed a Training Dashboard to streamline design and verification onboarding for freshers and lateral hires.

NXP Semiconductors *(Feb 2017 – May 2021)*
Head of Digital IP Design & Verification (MSIP Team)

- Built and led the MSIP Digital IP team, managing design and verification sign-offs for advanced digital IPs, including FIR/CIC filters and ADC/TempSense/Clocking interfaces for automotive and consumer devices.
- Delivered ISO 26262-compliant designs, integrating DFT, test, and safety features for high-reliability applications.
- Developed state-of-the-art UVM testbenches & VIPs, ensuring functional, GLS, and AMS unified verification sign-off with traceability from requirements to test specifications.

KFAxx Series (Dec 2015 – Jan 2017)
Portfolio Verification Lead/Manager

- Led a 22-member verification team, overseeing four parallel device verifications with seamless knowledge-sharing across projects.
- Ensured logic freeze and tapeout sign-off while optimizing resource management for peak project demands.
- Directed pre-silicon emulation using Palladium, driving debug support and feature validation ahead of chip deployment.
- Collaborated with test engineering to develop cost-effective test strategies and ensure seamless qualification.

Rayleigh Project (Jan 2015 – Nov 2015)
Verification Lead

- Managed a 24-member team, driving on-time logic freeze & first-pass silicon qualification.
- Defined and implemented advanced verification methodologies for debug, platform, low-power, and security subsystems.
- Spearheaded pre-silicon verification on Palladium, ensuring robust test coverage for boot and security features.

Faraday Project (Jun 2013 – Dec 2014)
Senior Staff Engineer (Verification Lead)

- Led a 20-member team, overseeing high-performance verification of dual-core (ARM A5 + M4) processors for automotive and industrial applications.
- Defined comprehensive verification strategies, ensuring on-time tapeout and first-pass silicon success.

Halo1.0/2.0 (Jan 2011 – May 2013)
Verification Lead

- Led 12-member team verifying instrument cluster SoCs with ARM A5/M4 cores, dual TFT display, HUD warping engine, and advanced graphical interfaces.
- Defined debug architecture integration, ensuring seamless SoC-level verification.

Rainbow1.0/2.0 (Jan 2009 – Dec 2010)
Verification Lead

- Managed 12-member team, delivering next-gen 32-bit microcontrollers with PowerPC-based TFT instrument cluster solutions.
- Led verification closure, ensuring compliance with automotive-grade quality standards.

Spectrum Project (Jan 2007 – Dec 2008)
Principal Lead Engineer

- Led 8-member verification team, delivering PowerPC-based automotive microcontrollers with advanced graphics and cluster integration.
- Implemented CPF methodologies to achieve low-power verification sign-off.

UWB/Broadway Project (Sept 2006 – Dec 2006)
Verification Lead Engineer

- Managed 4-member team, integrating multi-language testbench environments for a multi-core SoC featuring 5 NIOS processors.
- Led verification for multiple IPs, including HSDI, MCIF, UART, SDIO, and SPI.

SCM/Zeus Project (Jan 2005 – Aug 2006)
Verification Lead Engineer

- Led front-end integration of a digital baseband processor using Rabbit.
- Verified the Security Module at RTL and gate level using VCS, ensuring compliance with design specifications.

Neptune_LTE90 / LTE2C90 / VLT Project (Jul 2003 – Dec 2004)
Senior Verification Engineer

- Verified key modules (WDOG, DTIMER, LEM, DSIH) across RTL, post-layout, and production environments.
- Developed ARM and DSP testbench environments in Assembly and C, optimizing functional validation.

Neptune_LTX / ULS Project (Aug 2002 – Jun 2003)
Senior Verification Engineer

- Led weekly testbench releases, database integration, and debug support for a global team.
- Established a production simulation environment using RESIM, improving verification efficiency.

Patriot_Indy Project (Sep 2001 – Jul 2002)
Verification Engineer

- Verified the GPIO Module, developing comprehensive test cases in Verilog and C.
- Conducted RTL, post-layout, and post-silicon debugging, ensuring design robustness.

Cheetal / Sika Project (Dec 1999 – Aug 2001)
Verification Engineer

- Enhanced RTL design for IPBUS peripherals, including RISC interface and interrupt controller.
- Automated regression testing and verified critical communication interfaces.

EDUCATION & CERTIFICATIONS

- **M. Tech (Microelectronics) from IIT-BHU**
- **B. Tech (ECE) from IIT-BHU**

TECHNICAL PROFICIENCY

- **Languages/Methodologies:** VHDL, Verilog, System Verilog, C, C++, Shell, Perl, TCL, UVM, Make
- **Tools:** IUS, VCS, LEC, HAL, IFV, Emgr, and certitude, Verdi
- **Others:** Clearcase, Design Sync
- **Methodologies:** SVBCL, UVM, ABV

PROFESSIONAL ENGAGEMENTS

- **University Relations**: Led NXP Campus Connect Program, intern mentorship, and fresher hiring
- **Technical Forums**: Speaker and contributor to semiconductor verification conferences

AWARDS & PUBLICATIONS

- 10 Publications | 3 Defensive Publications (In Progress) | 3 Patents Under Review
- Recipient of multiple internal awards for innovation and contributions to semiconductor verification.
- Pioneered the first-of-its-kind VPlan Automated Integration Traceability Flow with DOORS NG in the semiconductor industry.
  - **Presented at multiple international forums globally.**
  - **Featured in a video presentation: Watch Here.**
- Some links external publication links:
  - https://www.youtube.com/watch?v=-wCO6hHHg28
  - https://www.design-reuse.com/articles/35524/targeting-soc-address-decoder-faults-using-functional- patterns.html
  - https://www.design-reuse.com/articles/30668/benchmarking-an-arm-based-soc-using-dhrystone.html
  - https://dev.embedded.com/design/debug-and-optimization/4404213/Reducing-tester-based-silicon-debug- effort---time--Part-1---Testing-modes-