**1. Name and designation:**

**Dr. J. K. KASTHURI BHA, ASSISTANT PROFESSOR (Sr. G)**

kasthurj@srmit.edu.in

**2. Education** (Qualification starting from one acquired last)

| Degree | Discipline | Institution | Year |
|---|---|---|---|
| Ph.D. | Nano Electronics | SRM Institute of Science and Technology | 2021 |
| M. Tech | VLSI | SRM University | 2008 |
| B.E | ECE | V.R.S Engineering College, Affiliated to Madras University | 2001 |

**3. Academic Experience –**

**Total Number of Years: 21years 3 months (Till now)**

| Institution | Rank | Title | From | To | FT/PT |
|---|---|---|---|---|---|
| SRMIST NCR Campus | Sr. G | Assist. Professor | 19/05/2025 | Till Date | FT |
| SRMIST Kattankulathur Campus | Sr. G | Assist. Professor | 1/07/2017 | 18/05/2025 | FT |
| SRM University | O.G | Assist. Professor | 1/06/2009 | 30/06/2017 | FT |
| SRM University | | Lecturer | 27/01/2005 | 27/01/2005 | FT |

**4. Thesis Title**

| Field | Title | Guide Name | From | To | FT/PT |
|---|---|---|---|---|---|
| Nano Electronics | Design and Analytical Modeling of Multi-Gate FinFET towards Analog Application | Dr. P.Aruna Priya | 27/05/2014 | 18/06/2021 | PT |

**5. Current Membership in professional organization**

| Sl. No | Membership details |
|---|---|
| 1 | Indian Society for Technical Education (LM99014) |
| 2 | M-234000_Life Member in IETE |

**6. Honors and awards : -**

| Sl. No | Nature of honour/award |
|---|---|
| 1 | Implementation of Optimized Multiplier Using Vedic Sutra and Reversible Logic at the 45$^{th}$ Mid-Term Symposium at 4$^{th}$ &5$^{th}$ April 2014. |

**7. Principal publications of the last five years (2011 – Till Date)**

| Sl. No | Details of Journal publication |
|---|---|
| | |

| Sl. No | Details of Journal publication |
|---|---|
| 1. | Jiavana, K.F.**J. K. Kasthuri Bha**, Murugapandiyan, P. et al. Performance Comparison of GaN-based HEMTs on β-Ga2O3 Substrates Using Compositionally-Graded InGaN and AlGaN Back Barriers for High Frequency Applications. Semiconductors 60, 100–113 (Feb. 2026). https://doi.org/10.1134/S106378262560353X |
| 2. | K. Ferents Koni Jiavana, **J. K. Kasthuri Bha**, S. Kayalvizhi , and Ramkumar Natarajan, "Comparative Analysis of In0.15Ga0.85N and β-Ga2O3 Back Barriers in β-Ga2O3-Buffered AlGaN/GaN HEMT Structures for High-Speed RF Electronics", . Phys. Solid State 68, 50–63 (Feb. 2026). https://doi.org/10.1134/S1063783425603339 |
| 3. | Sannakashappanavar, B.S., Venkatasubbaiah, G., **J. K. Kasthuri Bha,** " Study of ohmic contact at Ti/ZnO interface by using electrical characteristics and KPFM analysis", Discover Materials 5, 175 (Sep.2025). https://doi.org/10.1007/s43939-025-00375-8 |
| 4. | **Kasthuri Bha, J. K**.; Aruna Priya, P, "Analysis of Under lap Tri-Gate FinFET and its Capacitance Effects for Analog/ Radio Frequency Applications", Journal of Nanoelectronics and Optoelectronics, Volume 18, Number 9, September 2023, pp. 1037 |
| 5. | **J. K. Kasthuri Bha**, K. Ferents Koni Jiavana, S. Kayalvizhi, "Low Complex Fractional-order Differentiators and Integrators" NeuroQuantology, Volume 20, Issue 6, Page 2114-2118, doi: 10.14704/nq.2022.20.6.NQ22205 |
| 6. | Vidhyadharan, A.S., **Kasthuri Bha, J K**. & Vidhyadharan, S. "CNTFET-based Ultra-Low-Power Dual-VDD Ternary Half Adder". Circuits Systems and Signal Processin 40, 4089–4105 (2021) https://doi.org/10.1007/s00034-021- |
| 7. | **J.K.Kasthuri Bha**, P.Aruna Priya, "Low Power and High Gain Differential Amplifier using 16 nm FinFET," in Microprocessors and Microsystems, Vol. 71, Nov. 2019. (SCI -1.045) https://doi.org/10.1016/j.micpro.2019.102873 |
| 8. | J.K.Kasthuri Bha, P. Aruna Priya, "10 nm Trigate High k Underlap FinFETs: Scaling Effects and Analog Performance," in Silicon, Dec. 2019 (SCI-E -1.281) https://doi.org/10.1007/s12633-019-00299-y |
| 9. | **J.K.Kasthuri Bha et.al** ,"Design optimization of Vedic multiplier using Reversible Logic", International journal of Engineering Research and Technology,volume 3,Issue.03,March-2014 https://www.ijert.org/research/design-optimization-of-vedic-multiplier-using-reversible-logic-IJERTV3IS031946.pdf |
| 10. | J.K.Kasthuri Bha **et.al**,"Design of digital configurable error free frequency detector using strobe signal", International journal of Engineering Research and applications volume 4, Issue.04, April 2014 http://www.ijera.com/pages/v4no4(v2).html |
| 11. | J.K.Kasthuri Bha **et.al** ,"A novel high performance junction less FinFET International Conference on Nano science and Nanotechnology-2015and published", International Journal of ChemTech Research vol 07 2014-2015 https://sphinxsai.com/2015/ch_vol7_no2_ICONN/8/NF01%20(1027-1031).pdf |
| 12. | Charan Teja, J**. K.Kasthuri Bha**, P.Aruna Priya, D.John Thiruvadigal," Design of FinFET Based LNA with reduction of Corner Effects", International Journal of ChemTech Research, Volume 7, Issue 2, pp.867-873, Feb 2015 https://sphinxsai.com/2015/ch_vol7_no2_ICONN/6/NE07(867-873).pdf |
| 13. | Swetha D,**J. K.Kasthuri Bha**, P.Aruna Priya, D.John Thiruvadigal," Modelling of Tri Gate FinFET s", International Journal of Chem Tech Research,Volume 7,Issue 2,pp. 892-896 Feb 2015 https://sphinxsai.com/2015/ch_vol7_no2_ICONN/6/NE12%20(892-896).pdf |
| 14. | **J.K.Kasthuri bha**,P.Aruna Priya "A Comparative study of Recessed strap Dopant Segregated Schottky and SYM-K SPACER FinFET" International journal of control theory and application volume 9 issue 15, 2016, pp. 7395-7400 https://serialsjournals.com/abstract/17006_51.pdf |

| Sl. No | Details of Journal publication |
|---|---|
| 15. | **J. K. KasthuriBha**, Sushil S. Pardeshi and P. Aruna Priya "OOK Transmitter in DG FinFET Technology" International journal of control theory and application volume 9 issue 14, 2016, pp. 6361- 6366 https://serialsjournals.com/abstract/89335_3.pdf |
| 16. | Pronoy sinha, **J.K.Kasthuri Bha**" Improved SRAM Cell using FinFET in Terms of Power and Stability" International journal of control theory and application volume 9 issue 13, 2016, pp. 6301-6307 |
| 17. | **J.K.Kasthuri Bha**,Avikmajumdar,"A fast Locker all-digital delay locked loop using a register controlled technique International journal of VLSI & Embedded systems Vol 05pg no.785-793 Article 03242 ISSN 2249-6556 |

| Sl. No | Details of Conference publication |
|---|---|
| 1 | Jai Surya, J.K.Kasthuri Bha, "Real-Time and Energy-Efficient Ship Detection using YOLOv8 on FPGA Platforms for Maritime Surveillance"RAEEUCCI -2025 SRMIST April 23rd to April 25, India |
| 2 | Vishal Kumar, Abhinav Mishra, Sparsh Goyal and Kasthuri Bha J.K, "32 bit RISC-V Processor with Switchable floating point ALU" IEEE 5th International Conference on VLSI Systems, Architecture, Technology and Applications (VLSI SATA)2025 |
| 3 | Kasthuri Bha J, K, "A Comprehensive Parametric Analysis on Device Linearity and Mathematical Modeling of Nanoscale Multi-Gate FinFET, Tailored for Cutting-Edge Analog Applications" ICONN 2025 India |
| 4 | Kasthuri Bha J K, "Design of Low Power Ambipolar CNTFET-based Digital Adders", 9th International Conference on Nano electronics, Computational Intelligence & Communication Systems (NCCS-2023) organized by ISVE Ranchi at Advanced Regional Telecom Training Centre, BSNL, , India during April 13 -14th , 2024 |
| 5 | Rakesh Yerragoppu, Aruna Priya P, Kasthuri Bha J K, "Modeling, optimization and comprehensive comparative analysis of 7nm FinFET and 7nm GAAFET devices", AIP Conference Proceedings 2277, 020003 (2020); |
| 6. | J. K. Kasthuri Bha, P. Aruna Priya, "Analysis and Design of FinFET Based Tunable Amplifier," in International Conference on Nano science and Nanotechnology, 9-11th August 2017, India. |
| 7. | J.K.Kasthuri Bha,P.Aruna Priya,"Power Optimization of RF Transceiver with cascade low noise amplifier using FinFET,5th IEEE International conference on communications and signal Processing" April 6,2016 |
| 8. | J.K.Kasthuri Bha, P.Aruna Priya "A Comparative study of Recessed strap Dopant Segregated Schottky and SYM-K SPACER FinFET" the Joint International Conference On Artificial Intelligence and Evolutionary Computations in Engineering Systems (ICAIECES-2016) & Power, Circuit and Information Technologies (ICPCIT-2016) 19-21 May 2016. |
| 9. | J.K.Kasthuri Bha ,"A New approach to Eddr using Rq Code ",International conference on computer science and Engineering held at pune on 17th March 2013 |
| 10 | J.K.Kasthuri Bha ,"FPGA implementation of 32-bit CSLA using BEC", International conference on computer science and Engineering held at pune on 17th March 2013 |

1. **Patents**

| | |
|---|---|
| Patent application no. | 202023100243 |
| Date | 3rd February 2023 |

| | |
|---|---|
| Title | A PREDICTIVE MODEL OF ACCIDENTS USING MACHINE LEARNING ALGORITHM |
| Inventors | Himma Bindhu, Kasthuri Bha J K, Ferents koni Jiavana, Kayalvizhi S |

- **Details of Courses, Conferences, Workshops, Seminars, etc. attended**

| Sl. No | Details of Courses, Conferences, Workshops, Seminars |
|---|---|
| 1 | Online Training Programme on "NEP 2020 Orientation & Sensitization Programme" (06th February – 14th February, 2026) under Malaviya Mission Teacher Training Programme (MMTTP) of University Grants Commission (UGC) |
| 2 | 5- Days Employee Development Program (EDP) on "Emerging Trends in Quantum Computing, Artificial Intelligence, and Advanced Technologies", organized by the School of Electronics Engineering (SENSE), VIT-AP University, Amaravati, held from 27- 31 January 2026. |
| 3 | Faculty development Programme on Cryogenic Electronics for Quantum Computing IIT Chennai 2025 |
| 4 | Faculty development Programme on " Introduction to Quantum Computing: Quantum Algorithmn and Qiskit IIT Chennai 2025 |
| 5 | 8-day Face-to-Face UHV-II FDP organized by All India Council for Technical Education (AICTE) at S.R.M. Institute of Management and Technology, Modinagar, Ghaziabad from 27th June to 4th July 2025 |
| 6 | One week Internship & training on "Quantum Computing with Machine Learning organized by EDUX Labs in association with Mechanica IIT Madras 02/06/2025 to 06/06/2025 |
| 7 | Faculty development Programme on Introduction To Machine Learning IIT Chennai 2024 |
| 8 | Faculty development Programme on AI_ Knowledge Representation And Reasoning, IIT Chennai 2024 |
| 9 | 5 days Faculty development program on 5th edition Patent school workshop from 19th September to 23rd September 2023 in SRMIST Kattankulathur |
| 10 | Six days Professional development Program on, " Recent Advancements in organic and Nano electronics" RAONE 2023 |
| 11 | Professional development Program on Verilog Programming from 13/06/2022 to 17/06/2022 Verilog Programming, National Institute of Technical Teachers Training and Research Chennai |
| 12 | Insight of Analog and Digital IC Design : Overview of VLSI Tools (IADICD - 2022) 14th - 19th November 2022 |
| 13 | ATAL workshop on Intellectual property rights on Academia: Criterion Protection and cialization, February 7th to 11th 2022, Andhra University |
| 14 | Attended 5 days workshop on "Examination Reforms" during Mar 20 to Mar 26, 2021 |
| 15 | Semiconductor Devices and Circuits "Recent Advancements in Organic & Nano Electronics-RAONE-21" |
| 16 | Two_day hands on Training on MIT-MEEP |
| 17 | D3-Gui based FPGA Programming 20th-24th December 2021, Srmist, Vadapalani |
| 18 | LI-FI Technologies and Applications April 13th-22nd , 2021 |
| 19 | Recent Advancements in Organic & Nano Electronics-RAONE-20 |
| 20 | Attended 5 days International workshop on "Evolution of Electronic structure theory and Experimental Realization 11-15 September 2018 at SRMIST & IITM, India |
| 21 | Attended two days workshop on Modelling Semiconductor Device at Nano scale held on 8-9 September 2016 |
| 22 | Workshop on Multicarrier Modulation Techniques, 18th October 2010, SRM Institute of Science and Technology (formerly known as SRM University), Kattankulathur. |
| 23 | One day Faculty Symposium on MIMO-OFDM Wireless Systems, 27th January 2011, Dept. of ECE, |

| | |
|---|---|
| | SRM Institute of Science and Technology (formerly known as SRM University), Kattankulathur |
| 24 | Two-week ISTE Workshop on Basic Electronics, 28th June to 8th July 2011, Indian Institute of Technology, Bombay |
| 25 | FDP on Advanced VLSI Design, 17th to 19th November, 2011, SSN College of Engineering, kalavakkam |
| 26 | Two day Short term training program on MI MO-Communications and Networks, February 1st – 2nd ,2012, SRM Institute of Science and Technology (formerly known as SRM University), Kattankulathur |
| 27 | Two day ISTE workshop on writing effective conference papers, Indian Institute of Technology, Bombay on 18th & 19th |
| 28 | One day Synopsis University Symposium on 2014 custom IC design |

- **Details of Online Courses completed**

| | |
|---|---|
| 1 | NPTEL: Introduction to Quantum Computing: Quantum Algorithm and Qiskit |
| 2 | NPTEL: Cryogenic Electronics for Quantum Computing |
| 3 | NPTEL: VLSI Physical Design with Timing Analysis |
| 4 | NPTEL: AI_ Knowledge Representation And Reasoning |
| 5 | NPTEL: Introduction To Machine Learning |
| 6 | NPTEL:Artificial Intelligence _ Search Methods For Problem solving |
| 7 | Advanced ARM SoC Design (National Institute of Electronics and Information Technology (NIELIT), |
| 8 | ARM Based SoC Design (National Institute of Electronics and Information Technology (NIELIT) |
| 9 | NPTEL_System Design Through VERILOG |
| 10 | NPTEL: Physics of Nanoscale Devices |
| 11 | NPTEL: CMOS Digital VLSI Design; |
| 12 | NPTEL Semiconductor Devices and circuits |
| 13 | NPTEL: Design thinking A Premier |
| 14 | Introduction to Quantum Information –Korea Advanced Institute of Science and Technology (KAIST) |
| 15 | Python for Data science, AI & Development IBM |
| 16 | Getting started with AI using IBM Watson |
| 17 | Building AI Powered Chat-bots Without Programming –IBM |
| 18 | Introduction to Artificial Intelligence |

**Personal Details**

**Name:** J.K.Kasthuri Bha
**Gender:** Female
**Date of Birth :**14/02/1980 Age:45
**Husband Name:** Vinoth Kumar S
**Address for communication:**
E904, Rajnaar Residency, Rajnagar Extension Ghaziabad
**Mail ID:** kasthuriroshan@gmail.com
**Contact Number:** 9444514835

**The details given above is True to the best of my knowledge**

**Yours Faithfully**