FACULTY PROFILE

Name: Dr. Minakshi Sanadhya

Designation: Assistant Professor

E_Mail: minakshs@srmist.edu.in

Professional Qualification:

- Ph.D. (Digital Circuit Design)
- M.Tech. (VLSI Design)
- B.E.(Applied Electronics & Instrumentation)

Journals Publications:

- Sanadhya M. and Sharma D.K. "Adiabatic Logic Based Energy Efficient Architecture of 1 - Bit Magnitude Comparator for IOT Applications", Journal of Internet Technology, Vol.23 (7), pp.1643-1649, 2022.
- Sanadhya M. and Sharma D. K., "Adiabatic Logic- Based Shift Registers for Low Energy IOT Architecture—Design and Contemplation," IET Communication, pp. 1-9,2022.
- Sanadhya M. and Sharma D. K., "Low Power Architecture of Logic Gates Using Adiabatic Techniques," Indonesian Journal of Electrical Engineering and Computer Science, 25(2), pp. 805-813, 2022.

- Sanadhya M. and Sharma D. K, "D Flip-Flop Design by Adiabatic Technique for Low Power Applications", Indonesian Journal of Electrical Engineering and Computer Science, 29(1), pp. 141-146, 2022.
- Sanadhya M. and Sharma D. K, "Adiabatic Technique Based Low Power Synchronous Counter Design," International Journal of Electrical and Computer Engineering, 13(4), pp.3770-3777,2023 .
- Pradhan L. M. and Sanadhya M., "Adiabatic Power Gated Circuits to Reduce Leakage Implementing a Mode 6 Counter", IJIR, 2(8), pp. 1209-1212, 2016
- Dhawan I, Ghosh R. and Sanadhya M., "Design Of Module-Integrated Isolated Solar Micro inverter Without Electrolytic Capacitors",IJESRR 3(2), pp. 141-144, 2016.
- Tyagi V. and Sanadhya M., "Effectuation of USB 3.0 Super Speed Physical Layer Using Verilog HDL", IJARETS , 2(3), pp.65-70, 2015.
- Kumar A. Sanadhya M. and Singh N., "High Performance Circuit Level Design For Multiplier", IJARCSSE, 2(5), 2012.
- Sanadhya M., Kumar A. and Vishnoi M., Design Of An Efficient 16-Bit Microprocessor Using VHDL, IJESR, 2(8), pp.843-853, 2012.
- Singh N., Singh D. and Sanadhya M. "Command Mode Decoding Logic for Bus Management Unit", IJSCE, 2(3), pp. 415-419, 2012.
- Vishnoi M., Kumar A. and Sanadhya M., "Design of Improved Built-In-Self-Test Algorithm (8n) for Single Port Memory" ,IJSCE, 2(5), pp. 281-285, 2012.

Conference Publications

- Sanadhya M. and Sharma D. K., "Design and Implementation of Full Subtractor using
- Different Adiabatic Techniques," Proc. 2020 IEEE International Woman in Engineering
- Conference on Electrical and Computer Engineering,Bhubaneswar, India, pp. 102-106,
- 2021.
- Sanadhya M. and Sharma D. K., "Design of Low Power and High-Speed 6-Transistors Adiabatic Full Adder," Proc. Fifth International Conference on Information and Communication Technology for Competitive Strategies, Jaipur, India, Lecture Notes in Networks and System, pp. 795 -801, 2021.
- Sharma A.B., Lamba OS. ,Sharma A. and Sanadhya M. ,"Investigation to Measure Risk Free Exposure from Mobile Base Station Antennas in Residential Area", Proc. Second International Conference on Micro-Electronics and Telecommunication Engineering, Modinagar, pp.64-70, 2018.
- Sanadhya M., "A Novel Low Power High Speed 8 Transistor 1 –bit Adiabatic Full Adder Cell" Presented on Research Day at SRM University, Chennai, on 29 Feb 2016.

- Sanadhya M. and Kumar M.V., "Recent development in efficient adiabatic logic circuits and power analysis with CMOS logic" Proc. Third international conference on recent trend in computing, Modinagar, pp. 1299-1307, 2015.
- Sanadhya M.,"High performance circuit level design of digital FIR Filter" Proc. International conference RG education society, 2011.
- Sanadhya M.,"Design of 4-point FFT Processor an asynchronous and synchronous", Proc. National conference, Kota,2011.

Book Chapter

- Sanadhya M. and Sharma D. K., "Study of Adiabatic Logic Based Combinational and Sequential Circuits for Low Power Applications," in Low power Architecture for IoT Applications, Springer Tracts in Electrical and Electronics Engineering,2023.

Patent

- Patent Application No. : 202241030171 A "A machine learning based system for physical attack protection for VLSI Chip level hardware security and method thereof", published on June 03, 2022.

Awards and Achievements

- Gold Medalist in Post Graduate Degree , 2010
- Elite Certificate from NPTEL Course in Digital Circuits in Year 2018
- Elite Certificate from NPTEL Course in Microprocessors and Microcontrollers in Year 2019

Workshops/Seminars/FDPs

- Attended a three days Faculty Development program on "Inculcating Universal Human Values in Technical Education" at SRMIST Delhi –NCR Campus from 30 May- -1 June 2024.
- Attended a ten days Faculty Development program on NEP 2020 Orientation & Sensitization Programme under Malaviya Mission Teacher Training Programme (MM-TTP) of University Grants Commission (UGC) at Indian Institute of Information Technology, Design and Manufacturing, Kancheepuram, Chennai from 2-11 January 2024.
- Attended in a six days Faculty Development program on advance MATLAB programming with applications in engineering technology at SRMIST Delhi –NCR Campus from 12-17 June 2023.
- Attended a six days Faculty Development program on IoT and wearable device for smart City infrastructure at SRMIST Delhi –NCR Campus from 20-25 June 2022.

- Attended a six days Faculty Development program on Wearable Devices for IoT and Microwave Infrastructure at SRMIST Delhi –NCR Campus from 20-25 Dec. 2022.
- Attended a one week Faculty Development program on advance security analytics and machine learning at SRMIST Delhi –NCR Campus from 18-24 April 2022.
- Attended a one week Faculty Development program by AICTE Training and Learning (ATAL) Academy on "Nano Electronics and RF Engineering" at SRMIST, Delhi- NCR Campus from 6-10 September 2021.
- Attended a online national level Faculty development program on decoding examination which is organized by skillslate held on 8 May 2020.
- Attended a one day workshop on the Research Writing and Software Assisted Data Analysis, held at SRMIST , on 28 February 2020.
- Attended a three days Faculty Development program on Natural language processing using machine learning at SRMIST Delhi –NCR Campus from 27-29 June .2019.
- Attended three day National Seminar on the applications of technical terminology in modeling, optimization and computing in science and technology, the title of the lecture is vibhin adiabatic technology ka upyog kerke inverter ka pardarshan vishleshon held at SRMIST, 26-28 April 2019.
- Attended a Two Week Multidisciplinary Faculty Development Program EURDITIA from 12-23 June 2018
- Attended Faculty Development Program On Entrepreneurship which is sponsored by DST held during 14-28 June 2018.
- Attended a RF/Microwave design and simulation workshop on September 2018.
- Attended a three days Faculty Development Program on "Entrepreneurship Development", at SRM University, Ghaziabad, on 3 – 5 November 2015.
- Attended a Faculty Development Program on "Teaching Ethics "held at SRM University , on 24th January 2014.
- Attended one week short course on E-governance ,Eco –preneurship and Gution through ICT ",Organized by national Institute of technical Teachers Training and Research, Chandigarh (MHRD,Govt.of India),9-13 February,2015
- Attended Guest lecture on Application of Microwave in Material and Mineral Technology on March 29th , 2016
- Organized a National Conference on Recent Trends in Information & Communication Technology at SRM University on September 2013.

- Attended a One day seminar on wireless & telecom (CETPA) at SRM University on February 2014.
- Attended One day workshop on ARM Processor (CETPA) at SRM University on August 2014.
- Attended One day workshop on Panasonic PLC's (CETPA) at SRM University on March 2015.

Work Experience:

- Senior Lecture, Gurukul Institute Of Engineering And Technology, Kota(Raj.), April – June,2010.
- Assistant Professor, Electronics and Communication Engineering Department, SRM institute Of Science and Technology,2010 onwards

Professional Memberships:

- Member of International Association of Engineers- 155519
- Associate Member of Institution of Engineers- AM1631430
- Life Member of the Indian Society for Technical Education (ISTE)- 137334