

1. Name and designation	Dr. J. K. KASTHURI BHA, ASSISTANT PROFESSOR (Sr. G)
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2. Education (Qualification starting from one acquired last)

Degree	Discipline	Institution	Year
Ph.D.	Nano Electronics	SRM Institute of Science and Technology	2021
M. Tech	VLSI	SRM University	2008
B.E	ECE	V.R.S Engineering College, Affiliated to Madras University	2001

3. Academic Experience –

Total Number of Years: 20years 6 months (Till now)

Institution	Rank	Title	From	To	FT/PT
SRMIST NCR Campus	Sr. G	Assist. Professor	19/05/2025	Till Date	FT
SRMIST Kattankulathur Campus	Sr. G	Assist. Professor	1/07/2017	18/005/2025	FT
SRM University	O.G	Assist. Professor	1/06/2009	30/06/2017	FT
SRM University		Lecturer	27/01/2005	7/05/2008	FT

4. Nonacademic experience

Company / entity	Title	Brief description of position	From	To	FT/PT

5. Thesis Title

Field	Title	Guide Name	From	To	FT/PT
Nano Electronics	DESIGN AND ANALYTICAL MODELING OF MULTI-GATE FINFET TOWARDS ANALOG APPLICATION	Dr. P.Aruna Priya	27/05/2014	18/06/2021	PT

6. Current Membership in professional organisations

Sl. No	Membership details
1	Indian Society for Technical Education (LM99014)
2	M-234000_Life Member in IETE

7. Honors and awards :-

Sl. No	Nature of honour/award
	Implementation of Optimized Multiplier Using Vedic Sutra and Reversible Logic at the 45 th Mid-Term Symposium at 4 th & 5 th April 2014.

8. Service activities (2010-2015)

Sl. No	Nature of service	Institution where rendered	year
1			

9. Principal publications of the last five years (2011 – Till Date)

Sl. No	Details of Journal publication
1.	Kasthuri Bha, J. K.; Aruna Priya, P, “Analysis of Under lap Tri-Gate FinFET and its Capacitance Effects for Analog/ Radio Frequency Applications”, Journal of Nanoelectronics and Optoelectronics, Volume 18, Number 9, September 2023, pp. 1037
2.	J. K. Kasthuri Bha, K. Ferents Koni Jiavana, S. Kayalvizhi, “Low Complex Fractional-order Differentiators and Integrators” NeuroQuantology, Volume 20, Issue 6, Page 2114-2118, doi: 10.14704/nq.2022.20.6.NQ22205
3.	Vidhyadharan, A.S., Kasthuri Bha, J K. & Vidhyadharan, S. “CNTFET-based Ultra-Low-Power Dual-VDD Ternary Half Adder”. Circuits Systems and Signal Processin 40, 4089–4105 (2021) https://doi.org/10.1007/s00034-021-
4.	J.K.Kasthuri Bha, P.Aruna Priya, “Low Power and High Gain Differential Amplifier using 16 nm FinFET,” in Microprocessors and Microsystems, Vol. 71, Nov. 2019. (SCI -1.045) https://doi.org/10.1016/j.micpro.2019.102873
5.	J.K.Kasthuri Bha, P. Aruna Priya, “10 nm Trigate High k Underlap FinFETs: Scaling Effects and Analog Performance,” in Silicon, Dec. 2019 (SCI-E -1.281) https://doi.org/10.1007/s12633-019-00299-y
6.	J.K.Kasthuri Bha ,”Design optimization of Vedic multiplier using Reversible Logic”, International journal of Engineering Research and Technology,volume 3,Issue.03,March-2014 https://www.ijert.org/research/design-optimization-of-vedic-multiplier-using-reversible-logic-IJERTV3IS031946.pdf
7.	J.K.Kasthuri Bha,”Design of digital configurable error free frequency detector using strobe signal”, International journal of Engineering Research and applications volume 4, Issue.04, April 2014 http://www.ijera.com/pages/v4no4(v2).html
8.	J.K.Kasthuri Bha ,”A novel high performance junction less FinFET International Conference on Nano science and Nanotechnology-2015and published”, International Journal of ChemTech Research vol 07 2014-2015 https://sphinxesai.com/2015/ch_vol7_no2_ICONN/8/NF01%20(1027-1031).pdf
9.	Charan Teja, J. K.Kasthuri Bha, P.Aruna Priya, D.John Thiruvadigal,” Design of FinFET Based LNA with reduction of Corner Effects”, International Journal of ChemTech Research, Volume 7, Issue 2, pp.867-873, Feb 2015 https://sphinxesai.com/2015/ch_vol7_no2_ICONN/6/NE07(867-873).pdf
10.	Swetha D,J. K.Kasthuri Bha, P.Aruna Priya, D.John Thiruvadigal,” Modelling of Tri Gate FinFET s”, International Journal of Chem Tech Research,Volume 7,Issue 2,pp. 892-896 Feb 2015 https://sphinxesai.com/2015/ch_vol7_no2_ICONN/6/NE12%20(892-896).pdf
11.	J.K.Kasthuri bha,P.Aruna Priya ”A Comparative study of Recessed strap Dopant Segregated Schottky and SYM-K SPACER FinFET” International journal of control theory and application volume 9 issue 15, 2016, pp. 7395-7400

Sl. No	Details of Journal publication
	https://serialsjournals.com/abstract/17006_51.pdf
12.	J. K. KasthuriBha, Sushil S. Pardeshi and P. Aruna Priya “OOK Transmitter in DG FinFET Technology” International journal of control theory and application volume 9 issue 14, 2016, pp. 6361- 6366 https://serialsjournals.com/abstract/89335_3.pdf
13.	Pronoy sinha, J.K.Kasthuri Bha“ Improved SRAM Cell using FinFET in Terms of Power and Stability” International journal of control theory and application volume 9 issue 13, 2016, pp. 6301-6307
14.	J.K.Kasthuri Bha,Avikmajumdar,”A fast Locker all-digital delay locked loop using a register controlled technique International journal of VLSI & Embedded systems Vol 05pg no.785-793 Article 03242 ISSN 2249-6556

Sl. No	Details of Conference publication
1	Jai Surya, J.K.Kasthuri Bha, “Real-Time and Energy-Efficient Ship Detection using YOLOv8 on FPGA Platforms for Maritime Surveillance”RAEEUCCI -2025 SRMIST April 23 rd to April 25, India
2	Vishal Kumar, Abhinav Mishra, Sparsh Goyal and Kasthuri Bha J.K, “32 bit RISC-V Processor with Switchable floating point ALU” IEEE 5th International Conference on VLSI Systems, Architecture, Technology and Applications (VLSI SATA)2025
3	Kasthuri Bha J, K, “A Comprehensive Parametric Analysis on Device Linearity and Mathematical Modeling of Nanoscale Multi-Gate FinFET, Tailored for Cutting-Edge Analog Applications” ICONN 2025 India
4	Kasthuri Bha J K, “Design of Low Power Ambipolar CNTFET-based Digital Adders”, 9th International Conference on Nano electronics, Computational Intelligence & Communication Systems (NCCS-2023) organized by ISVE Ranchi at Advanced Regional Telecom Training Centre, BSNL, , India during April 13 -14 th , 2024
5	Rakesh Yerragoppu, Aruna Priya P, Kasthuri Bha J K, “Modeling, optimization and comprehensive comparative analysis of 7nm FinFET and 7nm GAAFET devices”, AIP Conference Proceedings 2277, 020003 (2020);
6.	J. K. Kasthuri Bha, P. Aruna Priya, “Analysis and Design of FinFET Based Tunable Amplifier,” in International Conference on Nano science and Nanotechnology, 9-11 th August 2017, India.
7.	J.K.Kasthuri Bha,P.Aruna Priya,”Power Optimization of RF Transceiver with cascade low noise amplifier using FinFET,5 th IEEE International conference on communications and signal Processing” april 6,2016
8.	J.K.Kasthuri Bha, P.Aruna Priya “A Comparative study of Recessed strap Dopant Segregated Schottky and SYM-K SPACER FinFET” the Joint International Conference On Artificial Intelligence and Evolutionary Computations in Engineering Systems (ICAIECES-2016) & Power, Circuit and Information Technologies (ICPCIT-2016) 19-21 May 2016.
9.	J.K.Kasthuri Bha ,”A New approach to Eddr using Rq Code “,International conference on computer science and Engineering held at pune on 17 th March 2013

Sl. No	Details of Conference publication
10	J.K.Kasthuri Bha ,”FPGA implementation of 32-bit CSLA using BEC”, International conference on computer science and Engineering held at pune on 17 th March 2013

Funded Project

1. Patents

Patent application no.	202023100243
Date	3 rd February 2023
Title	A PREDICTIVE MODEL OF ACCIDENTS USING MACHINE LEARNING ALGORITHM
Inventors	Himma Bindhu, Kasthuri Bha J K, Ferents koni Jiavana, Kayalvizhi S

• Details of Courses, Conferences, Workshops, Seminars, etc. attended

Sl. No	Details of Courses, Conferences, Workshops, Seminars
1	Faculty development Programme on Introduction To Machine Learning IIT Chennai 2024
2	Faculty development Programme on AI_ Knowledge Representation And Reasoning, IIT Chennai 2024
3	5 days Faculty development program on 5 th edition Patent school workshop from 19 th September to 23 rd September 2023 in SRMIST Kattankulathur
4	Six days Professional development Program on, “ Recent Advancements in organic and Nano electronics” RAONE 2023
5	Professional development Program on Verilog Programming from 13/06/2022 to 17/06/2022 Verilog Programming, National Institute of Technical Teachers Training and Research Chennai
6	Insight of Analog and Digital IC Design : Overview of VLSI Tools (IADICD - 2022) 14th - 19th November 2022
7	ATAL workshop on Intellectual property rights on Academia: Criterion Protection and cialization, February 7 th to 11 th 2022, Andhra University
8	Attended 5 days workshop on “Examination Reforms” during Mar 20 to Mar 26, 2021
9	Semiconductor Devices and Circuits “Recent Advancements in Organic & Nano Electronics-21”
10	Two_day hands on Training on MIT-MEEP
11	D3-Gui based FPGA Programming 20 th -24 th December 2021, Srmist, Vadapalani
12	LI-FI Technologies and Applications April 13 th -22 nd , 2021
13	Recent Advancements in Organic & Nano Electronics-RAONE-20

14	Attended 5 days International workshop on “Evolution of Electronic structure theory and Experimental Realization 11-15 September 2018 at SRMIST & IITM, India
15	Attended two days workshop on Modelling Semiconductor Device at Nano scale held on 8-9 September 2016
16	Workshop on Multicarrier Modulation Techniques, 18 th October 2010, SRM Institute of Science and Technology (formerly known as SRM University), Kattankulathur.
17	One day Faculty Symposium on MIMO-OFDM Wireless Systems, 27 th January 2011, Dept. of ECE, SRM Institute of Science and Technology (formerly known as SRM University), Kattankulathur
18	Two-week ISTE Workshop on Basic Electronics, 28 th June to 8 th July 2011, Indian Institute of Technology, Bombay
19	FDP on Advanced VLSI Design, 17 th to 19 th November, 2011, SSN College of Engineering, kalavakkam
20	Two day Short term training program on MI MO-Communications and Networks, February 1 st – 2 nd ,2012, SRM Institute of Science and Technology (formerly known as SRM University), Kattankulathur
21	Two day ISTE workshop on writing effective conference papers, Indian Institute of Technology, Bombay on 18 th & 19 th
22	One day Synopsis University Symposium on 2014 custom IC design

• **Details of Online Courses completed**

1	NPTEL: VLSI Physical Design with Timing Analysis
2	NPTEL: AI_ Knowledge Representation And Reasoning
3	NPTEL: Introduction To Machine Learning
4	NPTEL: Artificial Intelligence _ Search Methods For Problem solving
5	Advanced ARM SoC Design (National Institute of Electronics and Information Technology (NIELIT),
6	ARM Based SoC Design (National Institute of Electronics and Information Technology (NIELIT)
7	NPTEL_ System Design Through VERILOG
8	NPTEL: Physics of Nanoscale Devices
9	NPTEL: CMOS Digital VLSI Design;
10	NPTEL Semiconductor Devices and circuits
11	NPTEL: Design thinking A Premier
12	Introduction to Quantum Information –Korea Advanced Institute of Science and Technology (KAIST)
13	Python for Data science, AI & Development IBM
14	Getting started with AI using IBM Watson
15	Building AI Powered Chat-bots Without Programming –IBM
16	Introduction to Artificial Intelligence

Personal Details

Name: J.K.Kasthuri Bha

Gender: Female

Date of Birth :14/02/1980 Age:45

Husband Name: Vinoth Kumar S

Address for communication:

E904, Rajnaar Residency, Rajnagar Extension Ghaziabad

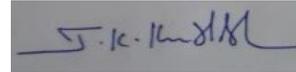
Mail ID: kasthurj@srmist.edu.in

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The details given above is True to the best of my knowledge

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Yours Faithfully

A rectangular box containing a handwritten signature in black ink. The signature appears to be "S.K. Kasthurj" written in a cursive style.